REMARKS

The claims have been amended to eliminate dependencies that are improper under U.S. practice.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account.

Respectfully submitted,

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marked-up claims

said basic cells and said power supply wirings are electrically connected.

16. A semiconductor device as claimed in claim 13 or 14, wherein at least one of a pair of semiconductor regions for source and drain of unused field effect transistors among said field effect transistors and said power supply wirings are electrically connected.

17. (Amended) A semiconductor device as claimed in [any one of claims 13 to 16], wherein said circuits are logic circuits and said switch elements are discretely arranged in said semiconductor substrate. (claim 13 or 14)

18. A semiconductor device as claimed in claim 16, wherein said unused field effect transistors are field effect transistors of basic cells not forming logic circuits and said unused basic cells are formed among said switch elements.

19. (Amended) A semiconductor device as claimed in [any one of claims 13 to 18], wherein said circuit comprising the switch elements is a clock circuit or a flip-flop circuit. (claim 13 or 14)

20. (Amended) A semiconductor device as claimed in [any one of claims 13 to 19], wherein said switch elements are formed of field effect transistors in said basic cells. (claim 13 or 14)

21. (Amended) A semiconductor device as claimed in any one of claims 7 to [20] 14, wherein said basic cells include the p-channel type field effect transistors and n-channel type field effect transistors.

(Amended)
22. A semiconductor device as claimed in any one of claims 7 to 12 [or 20], wherein a wiring electrically connected to the gate electrode of said switch element is formed of the wiring of the third wiring layer and this wiring is arranged in parallel to said power supply wirings.

(Amended)
23. A semiconductor device as claimed in any one of claims 7 to [22] 14, wherein a semiconductor region for power feeding to supply the predetermined voltage to the semiconductor region formed in said semiconductor substrate is formed in the region between the internal circuit region where a plurality of said basic cells are arranged and the peripheral circuit region at the external side of said internal circuit region.

24. A semiconductor device as claimed in claim 23, wherein a wiring for supplying the predetermined voltage to said semiconductor region for power feeding is arranged to surround said internal circuit region.

25. A semiconductor device as claimed in claim 24, wherein the wiring for supplying the predetermined voltage to said semiconductor region for power feeding is electrically connected to the terminal for testing via the external terminal of the semiconductor device.

26. A semiconductor device as claimed in claim 24, wherein the wiring for supplying the predetermined voltage to said semiconductor region for power feeding is electrically connected to the wiring for power

feeding arranged like a lattice within said internal circuit region.

27. (Amended) A semiconductor device as claimed in any one of claims 1 to [26] 14, wherein said switch elements are turned ON in the normal operation period of semiconductor device and the power supply voltage is applied from said power supply wirings to the semiconductor region formed in said semiconductor substrate and said switch elements are turned OFF in the testing or waiting period of semiconductor device and the voltage different from said power supply voltage is applied to said semiconductor region.

28. A semiconductor device, comprising:

a first semiconductor region formed in a semiconductor substrate;

a plurality of basic cells regularly arranged in said semiconductor substrate;

a first field effect transistor formed in said first semiconductor region as the field effect transistor of said basic cells;

a second field effect transistor formed in said second semiconductor region as the field effect transistor of said basic cells to have the conductivity type opposed to that of said first field effect transistor;

a first power supply wiring connected to said first field effect transistor;

(Amended)

37. A semiconductor device as claimed in claim 33, 34, or 35, wherein the wiring connected to the gate electrode of the field effect transistor forming said switch element is arranged to surround the internal circuit region of a semiconductor device.

(Amended)

38. A semiconductor device as claimed in any one of claims 33 to 37, wherein at least one of a pair of semiconductor regions for source and drain of the field effect transistors unused for said input/output circuits is electrically connected to said power supply wiring to form a capacitance element.

39. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming a switch element for electrically connecting or disconnecting the semiconductor region formed on said semiconductor substrate and the power supply wiring of the semiconductor device; and

(c) forming a plurality of circuits with the predetermined basic cells among a plurality of said basic cells.

40. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate;

(b) forming a switch element for electrically

predetermined circuit among a plurality of said circuits in said process (c).

42. A method of manufacturing a semiconductor device, comprising the processes of:

(a) regularly allocating a plurality of basic cells on a semiconductor substrate; and

(b) forming a plurality of circuits with the predetermined basic cells among a plurality of said basic cells,

wherein said switch element is built in the predetermined circuit among a plurality of said circuits.

43. A semiconductor device as claimed in claim 2, 4, 6 or 8, wherein a capacitance element is formed of said semiconductor region and a semiconductor region of the conductivity type opposed to that of said semiconductor region.

44. A semiconductor device as claimed in claim 3, 5, 9, 11 or 12, wherein a capacitance element is formed of said semiconductor region and at least one of a pair of semiconductor regions for source and drain of said unused field effect transistors.

45. (Amended) A semiconductor device as claimed in any one of claims 7 to 12[, 43 and 44], wherein a logic circuit is formed using said basic cells and said logic circuit is formed among the basic cells forming said switch element.

(Amended)
46. A semiconductor device claimed in claim 9, 11[,] or 12, 44 or 45; wherein a logic circuit is formed using said basic cells, said unused field effect transistor is the field effect transistor of basic cell not forming a logic circuit and said logic circuit and unused basic cells are formed among the basic cells forming said switch element.